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Korean Patent

1997-0051367

METHOD FOR OPTIMIZING WORD LINE VOLTAGE OF NONVOLATILE SEMICONDUCTOR MEMORY

[Bulwhibalsong Bandoche Memoriui Wodrain Jeonap Choijeokhwa
Bangbeop]

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Wodrain Jeonap Choijeokhwa
Bangbeop
English Title : METHOD FOR OPTIMIZING WORD LINE
VOLTAGE OF NONVOLATILE
SEMICONDUCTOR MEMORY

Specification

1. Title of the invention

METHOD FOR OPTIMIZING WORD LINE VOLTAGE OF NONVOLATILE
SEMICONDUCTOR MEMORY

2. Brief description of the figures

Figure 2 is a circuit diagram showing a block decoder and a cell array of an application example of the present invention.

Figure 3 is a flow chart for searching for an optimized word line voltage for reading data at a time of read in the present invention.

Figure 4 is a laser fuse block and a decoding circuit of the present invention.

Figure 5 is a voltage generating circuit diagram of the present invention.

Since this content is an important disclosure case, the text content has not been described.

¹ Numbers in the margin indicate pagination in the foreign text.

2. Claims

1. A method for optimizing a word line of a nonvolatile memory device, characterized by the fact that in a nonvolatile memory device, an optimum word line voltage level for reading data is detected and fixed by changing a control gate voltage that acts as a word line when data are read out.

2. The method for optimizing a word line of a nonvolatile memory device of Claim 1, characterized by the fact that the means for detecting the above-mentioned optimum word line voltage level programs all cells except for specific cells of a block, increases the word line voltage from the initial low voltage until the data are read out and the read data become specific data, and stores the increased times.

3. The method for optimizing a word line of a nonvolatile memory device of Claim 1, characterized by the fact that the means for fixing the above-mentioned detected optimum word line voltage level controls a word line voltage distributor so that its resistance value may be changed by a prescribed input signal in a circuit that applies a constant voltage to a reference voltage input terminal of a differential amplifier, applies a voltage distributed by the resistance to a load voltage input terminal, and obtains a specific word line voltage by

controlling a high voltage in which the output of the differential amplifier is a power supply or higher.

4. The method for optimizing a word line of a nonvolatile memory device of Claim 3, characterized by the fact that the above-mentioned prescribed input signal coding stores a prescribed input signal coding by a nonvolatile semiconductor memory itself or an external means, using one of laser, fuse, electrical fuse, and other devices that can store coding.

* Remarks: Disclosed according to the initially filed contents.

// Insert Figures 2-5 //

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Argument submission notice

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Title of the invention: NONVOLATILE SEMICONDUCTOR MEMORY DEVICE

As a result of examination of this filing, there are the following reasons for refusal, and they are notified according to the provisions of Article 63 of the Patent Law. If you have any arguments or need amendments, please submit the arguments (appended form No. 25-2 of the enforcement regulations of the Patent Law) and/or the amendments (appended form No. 5 form of the enforcement regulations of the Patent Law) until the above-mentioned submission date. (You can apply for an extension of the above-mentioned submission date at a unit of one month each time, and regarding this application, a separate extension approval will not be notified.)

(Reasons)

The invention described in Claims 1-19 of this application could have been easily invented as indicated as follows, prior to the filing of the patent application, by a person with ordinary skill in the art to which the invention pertains, a patent cannot be granted according to the provisions of Clause 2 of Article 29 of the Patent Law.

Claims 1-19 of the invention of this application are characterized by including a circuit that controls reading after reaching a fixed level and controls timing of a reading

operation in accordance with a control signal, when a power supply is raised to reduce the current consumption of a nonvolatile memory. However, the cited invention (Korean Laid-Open Patent No. 1997-51367) presents a technical constitution that is equipped with a circuit, which detects a voltage level while raising the voltage level when reading data to optimize the voltage of a nonvolatile memory, stores it, and controls an input voltage, and stores an input signal by fuse data, etc. Thus, the effects and the constitutions of two inventions are similar. Accordingly, the invention of the above-mentioned claims can be easily invented from the cited invention by a person with ordinary skill in the art to which the invention pertains.

(Attached document)

Attached document 1: Korean Laid-Open Patent No. 1997-51367

(July 29, 1997) 1 copy

End.

February 2, 2006

Korean Intellectual Property Office

Electronic Device Examination Team, Electric and Electronic
Examination Headquarter

Examiner, Ki-Hyeon Kim [seal]

<<Information>>

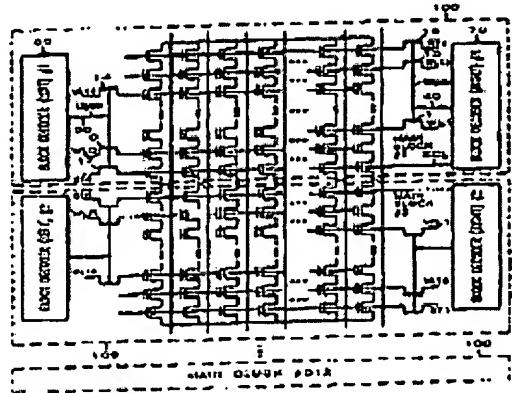
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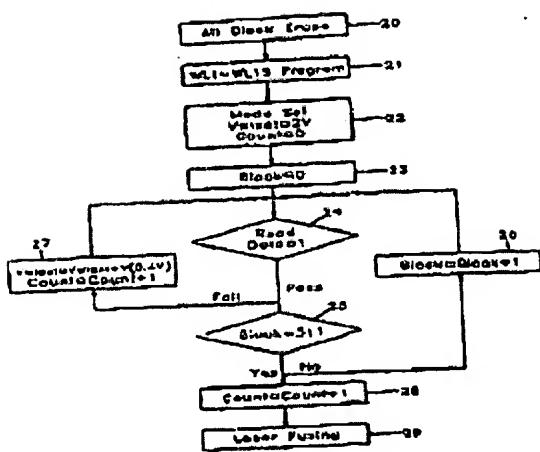
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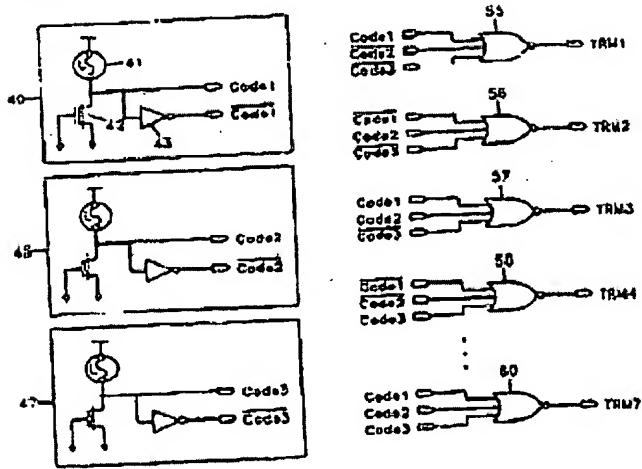
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